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MARTIN & ASSOCIATES, LLC			EXAMINER	
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CARTHAGE, MO 64836-0548				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/682,134

Applicant(s)

LUICK, DAVID ARNOLD

Examiner

Tonia L. Meonske

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-15 and 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9-15 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 9-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The rejection is maintained and provided below.

3. Referring to claim 9, the limitation "a register file bit comprising: a primary latch ... a plurality of secondary latches ..., a feedback path ... a context switch mechanism ..." is not clear. It is not understood how a single bit, which is merely a piece of information (see the definition of "bit" in Microsoft's Computer Dictionary, Fourth Edition, page 50 for support), can comprise hardware, such as the claimed latches, the feedback path and the context switch mechanism. A piece of information cannot comprise hardware. For the purposes of examination "a register file bit" is interpreted as "a register file". Appropriate correction is required.

4. Dependent claims 10-15 are rejected for incorporating the defects of independent claim 9.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 9-15 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Henry et al., US Patent 6,145,075 (Herein referred to as "Henry"). The rejections are respectfully maintained and copied below.

7. Referring to claim 9, Henry has taught an integrated circuit comprising:

- a. a register file bit (This is interpreted as a register file, see the 112 rejection above., Figure 5, element 506) comprising:
 - b. a primary latch (Figures 5 and 6, R1 in register file 306) having a data input (Figures 5 and 6, elements 550 and 552) and a data output (Figures 5 and 6, outputs from element 506 to elements 545 and 547);
 - c. a plurality of secondary latches (Figures 5 and 6, register file 306 (except for R1 which is the primary latch)) each having a data input (Figures 5 and 6, elements 550 and 552) and a data output (Figures 5 and 6, The outputs from element 506 to elements 545 and 547.);
 - d. a feedback path from the data outputs of the plurality of secondary latches to the data input of the first primary latch (Figures 5 and 6, At least elements 545, 547, 508, 510, 512, 513, 550, 552 and 560 comprise the feedback path.), the feedback path including a data selection mechanism for selecting one data output only from among each of the data outputs from the plurality of secondary latches to feed back to the data input of the first primary latch (column 6, line 40-column 7, line 47, Upon an exchange instruction, the data to be stored in R1 is selected only from among the registers in the register file, element 506.); and

- e. a context switch mechanism (abstract, Figure 5 is a mechanism that switches values in a microprocessor environment, or context. Figure 5 is the context switch mechanism.) that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches (column 6, line 40-column 7, line 47, Output from R1 is written to R2), and that causes the data on the data output of the selected one secondary latch to be written to the primary latch (column 6, line 40-column 7, line 47, Output from R2 is written to R1).
8. Referring to claim 10, Henry has taught the integrated circuit of claim 9, as described above and wherein the context switch mechanism comprises a swap gate control input on the primary latch (Figure 5, at least elements 541, 543, 540, 550 and 552).
9. Referring to claim 11, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches (Figure 5, At least elements 512, 513, 545, 547, 508, 510, 560, 550 and 552 each comprise the claimed delay element in the feedback path.).
10. Referring to claim 12, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises a delay element in the feedback path (Figure 5, At least elements 512, 513, 545, 547, 508, 510, 560, 550 and 552 each comprise the claimed delay element).

11. Referring to claim 13, Henry has taught the integrated circuit of claim 9, as described above, and wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch (column 6, line 40-column 7, line 47, column 8, lines 48-50, A clocked system latches data based on a clock signal. This is a clocked system, so the register data is latched through the system (input and output) based on the clock.) and at least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch (column 6, line 40-column 7, line 47, column 8, lines 48-50, A clocked system latches data based on a clock signal. This is a clocked system, so the register data is latched through the system (input and output) based on the clock.).

12. Referring to claim 14, Henry has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of write ports on the data input of the primary latch (Figure 5, elements 550 and 552 and ports carrying elements 541 and 543 comprise the claimed write ports.).

13. Referring to claim 15, Henry has taught the integrated circuit of claim 9, as described above, and further comprising a plurality of read ports on the data output of the primary latch (Figure 5, The ports carrying elements 545 and 547 comprise the claimed read ports.).

14. Referring to claim 21, Henry has taught a method for performing a fast context switch in a register file (Figure 5, element 506) that includes a primary latch (Figures 5 and 6, R1 in register file 306) and a plurality of secondary latches (Figures 5 and 6,

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register file 306 (except for R1 which is the primary latch)) having data outputs (Figures 5 and 6, The outputs from element 506 to elements 545 and 547.), the method comprising the steps of:

- (A) for a selected one secondary latch of the plurality of secondary latches, performing the steps of (A1) and (A2):
 - (A1) storing a first value in the primary latch that corresponds to a selected thread (column 7, lines 35-46, A value is stored in R1 in response to a selected process, or thread, containing an exchange instruction.);
 - (A2) moving the first value in the primary latch to the selected one of the plurality of secondary latches (column 2, lines 6-9, column 7, lines 35-47, R1 is moved to R2);
- (B) storing a second value in the primary latch that corresponds to an active thread (column 7, lines 35-46, A value is stored in R1 in response to an active process, or thread, containing an exchange instruction.);
- (C) selecting a data output of the selected one secondary latch only from among each of the data outputs of the secondary latches for performing a context switch with the primary latch (abstract, Figure 5 is a mechanism that switches values in a microprocessor environment, or context., column 6, line 40-column 7, line 47, Upon an exchange instruction, the data to be stored in R1 is selected only from among the registers in the register file, element 506. R1 is selected to be switched with R2.); and

(D) performing a context switch (abstract, Figure 5 performs a switch of values in a microprocessor environment, or context.) between the primary latch and the selected one secondary latch that causes the second value in the primary latch to be stored in the selected one secondary latch (column 2, lines 6-9, column 7, lines 35-47, R1 is stored in R2.), and that causes the first value in the selected one secondary latch to be stored in the primary latch (column 2, lines 6-9, column 7, lines 35-47, R2 is stored in R1.).

Response to Arguments

15. Applicant's arguments filed March 13, 2007 have been fully considered but they are not persuasive.

16. On page 6, Applicant argues with respect to claim 9 in essence:

"A register file bit as claimed herein is a portion of a register file. Each bit of the register file has a circuit as described and claimed herein as a "register bit". For example, a secondary thread "bit" is loaded into the primary latch 410 and then moved to the secondary latch 420 (See Figure 4 and page 5, line 26 through page 6 line 1). The latches 410 and 420 hold a single bit of the register file. Thus the register file bit is replicated to build a register file."

However, as explained above, it is not understood how a single bit, which is merely a piece of information (see the definition of "bit" in Microsoft's Computer Dictionary, Fourth Edition, page 50 for support), can comprise hardware, such as the claimed latches, the feedback path and the context switch mechanism. A piece of information cannot comprise hardware. Applicant's above argument even supports this by explaining that "a bit is loaded into a primary latch and then moved to a secondary latch...the latches hold a single bit..." This argument essentially states that a bit, or a piece of information, is loaded into a latch and

then moved to another latch, i.e. a piece of information is moved from one piece of hardware to another piece of hardware. A piece of hardware can comprise a piece of information, but a piece of information cannot comprise hardware. So claim 9 is indefinite for claiming a register file bit, or piece of information, comprising hardware. Therefore this argument is moot.

17. On pages 7 and 8, Applicant argues with respect to claims 9-15 and 21 in essence:

"However, Henry, and in particular the cited section does not teach or suggest anything concerning a plurality of secondary latches. In Henry there are only two latches – so a primary latch and a single secondary latch."

However, Henry has in fact taught a plurality of secondary latches. R1 in the register file is interpreted as the primary latch and all other registers in the register file are the plurality of secondary latches, where R2 specifies which register to select from among all of the registers in the register file. The register file necessarily contains more than the two registers specified by R1 and R2, otherwise there would be no reason to specify which registers to exchange in the instruction because the instruction would always exchange the same two register contents. So Henry has in fact taught a plurality of secondary latches (Figures 5 and 6, register file 306 (except for R1 which is the primary latch)). Therefore this argument is moot.

18. On page 8, Applicant argues with respect to claim 21 in essence:

"Henry does not teach or suggest a plurality of secondary latches and selecting one of the plurality of secondary latches for performing a context switch with the primary latch, as recited in claims 9 and 21."

However, Henry has in fact taught a plurality of secondary latches. R1 in the register file is interpreted as the primary latch and all other registers in the register file are the plurality of secondary latches, where R2 specifies which register to select from among all of the registers in the register file. The register file necessarily contains more than the two registers specified by R1 and R2, otherwise there would be no reason to specify which registers to exchange in the instruction because the instruction would always exchange the same two register contents. So Henry has in fact taught a plurality of secondary latches (Figures 5 and 6, register file 306 (except for R1 which is the primary latch)). Furthermore, the operand specifier R2 in an exchange instruction is used to select one of the plurality of secondary latches for performing a context switch with the primary latch (abstract, Figures 5 and 6, column 6, line 40-column 7, line 47). Therefore this argument is moot.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TLM



Tonia L. Meonske
May 22, 2007